UTILITY PATENT APPLICATION TRANSMITTAL

August 3, 2000

Attorney Docket No.:	CM03054J	Total Pages:	2
First-Named Inventor or Application Identifier	FREDERICK L. MARTIN		
Title:	DIGITAL-TO-PHASE-CONVERTER		
Express Mail Label No.:			

(Only for new nonprovisional applications under 37 CFR 1.53(b))

APPLICATION ELEMENTS (see MPEP chapter 600 concerning utility patent application contents)	*ADDRESS TO*:	Assistant Commissioner for Patents Box Patent Application Washington, D.C. 20231

1. [X] Fee Transmittal Form *in duplicate*
2. [X] Specification — *Total Pages* 12
3. [X] Drawings — *Total Sheets*: 4
4. [X] Oath or Declaration with Power of Attorney — *Total Pages* 3
   a. [X] Newly Executed (original or copy)
   b. [ ] Copy from prior application (37 CFR §1.63(d)) (for continuation/divisional with Box 17 completed)
      i. [ ] Deletion of Inventor(s): Signed statement attached deleting inventor(s) named in the prior application (see 37 CFR §1.63(d)(2) and 1.33(b)
5. [ ] Incorporation by Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. [ ] Nucleotide and/or Amino Acid Sequence Submission

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers *(cover sheet and document(s))*
9. [ ] 37 CFR §3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(should be specially itemized)*
14. [ ] Small Entity Statements

15. ☐	Certified Copy of Priority Document(s)
16. ☐	Other:

17. **IF A CONTINUING APPLICATION**
check appropriate box and supply the requisite information below and in a preliminary amendment:

☐ Continuation ☐ Divisional ☐ Continuation-in- Part (CIP) Prior Appl. No. _____

Prior Appl. information: | Examiner: | Group/Art Unit:

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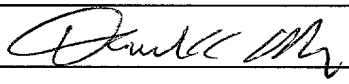
SIGNATURE			
DATE	August 3, 2000	Deposit Account User ID	13-4774-1740

PATENT

FEE TRANSMITTAL

Application Number	
Filing Date	
First-Named Inventor	FREDERICK L. MARTIN
Examiner Name	
Group/Art Unit	
Title:	DIGITAL-TO-PHASE-CONVERTER
Attorney Docket No.	CM03054J
TOTAL AMOUNT OF PAYMENT	**$730.00**

METHOD OF PAYMENT
(check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account No.	Deposit Account Name
13-4774	Motorola, Inc.

[X] Charge any additional Fee Required under 37 CFR § 1.16 and 1.17

[ ] Charge the Issue Fee set in in 37 CFR § 1.18 at the of the Mailing of the Notice of Allowance

FEE CALCULATION

1. BASIC FILING FEE

Large Entity

Code	Fee ($)	Fee Description	Fee Paid
101	690	Utility filing fee	$690
106	310	Design filing fee	
107	480	Plant filing fee	
108	690	Reissue filing fee	
114	150	Provisional filing fee	
Subtotal (1)			**$690**

FEE CALCULATION
(continued)

2. EXTRA CLAIM FEES

Claims			Extra Claims		Fee from Below		Fee Paid
Total		-20**	=	x		=	
Ind.		-3	=	x		=	
Multiple Dependent						=	

**or number previously paid, if greater; For Reissues, see below

Large Entity

Fee Code	Fee ($)	Fee Description
103	18	Claims in excess of 20
102	78	Ind. claims in excess of 3
104	260	Multiple dependent claim, if not paid
109	78	**Reissue independent claim over original patent
110	18	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)

FEE CALCULATION

(continued - next page)

Additional Fees (continued)		Large Entity	
Fee Code	Fee ($)	Fee Description	Fee Paid
105	130	Surcharge - late filing fee or oath	
127	50	Surcharge - late provisional filing fee or cover sheet	
139	130	Non-English specification	
147	2520	For filing a request for reexamination	
112	920*	Requesting publication of SIR prior to Examiner action	
113	1840*	Requesting publication of SIR after Examiner action	
115	110	Extension for reply within first month	
116	380	Extension for reply within second month	
117	870	Extension for reply within third month	
118	1360	Extension for reply within fourth month	
128	1850	Extension for reply within fifth month	
119	300	Notice of Appeal	
120	300	Filing a brief in support of an appeal	
121	260	Request for oral hearing	
138	1510	Petition to institute a public use proceeding	
140	110	Petition to revive - unavoidable	
141	1320	Petition to revive - unintentional	
142	1210	Utility issue fee (or reissue)	
143	430	Design issue fee	
144	580	Plant issue fee	
122	130	Petitions to Commissioner	
123	50	Petitions related to provisional applications	
126	240	Submission of IDS	
581	40	Recording each patent assignment per property	$40.00
		(times number of properties)	
146	690	Filing a submission after final rejection	
		(37 CFR § 1.129(a))	
149	690	For each additional invention to be examined	
		(37 CFR § 1.129(b))	
Other fee (specify)			
Other fee (specify)			
*Reduced by Basic Filing Fee		**Subtotal (3)**	**$40.00**

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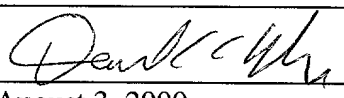
SIGNATURE			
DATE	August 3, 2000	Deposit Account User ID	13-4774-1740

DIGITAL-TO-PHASE-CONVERTER

TECHNICAL FIELD

This invention relates in general to electrical circuits, and more specifically to a digital-to-phase converter.

BACKGROUND

Current state of the art implementations of high-speed digital-to-phase converters for use in a frequency synthesis application provide approximately 40 megahertz (MHz) speed of operation and -40 dBc spurs (approximately 6-bit resolution) resolution. This is insufficient for most communication applications, where 1-gigahertz (GHz) operation and resolutions in the order of -80 dBc spurs are typical design benchmarks. A need thus exists in the art for a digital-to-phase converter that provides for improved resolution and speed.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the present invention, which are believed to be novel, are set forth with particularity in the appended claims. The invention, together with further objects and advantages thereof, may best be understood by reference to the following description, taken in conjunction with the accompanying drawings, in the several figures of which like reference numerals identify like elements, and in which:

FIG. 1 shows a block diagram of a digital-to-phase converter in accordance with the invention.

FIG. 2 shows a timing diagram showing the requirements for a synchronization circuit in accordance with the invention.

FIG. 3 shows timing diagram showing the time aperture divided into regions in accordance with the invention.

FIG. 4 shows a synchronization block for use with the digital-to-phase converter of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While the specification concludes with claims defining the features of the invention that are regarded as novel, it is believed that the invention will be better understood from a consideration of the following description in conjunction with the drawing figures, in which like reference numerals are carried forward.

Referring now to FIG. 1, there is shown a digital-to-phase converter (DPC) 100 in accordance with the invention. DPC 100 includes a tuned delay line 106 preferably using a delay-locked loop (DLL) with (N) equally spaced delay taps, a conventional multiplexor or selector circuit 108 and a synchronization circuit 110. Inputs to the DPC 100, in addition to supply and ground, are an n-bit ($n >= \log_2 N$) binary word (IN) 104, a binary reference clock (REF) 102 and a binary trigger signal (TRIG) 112. The circuit output is a single binary output signal (OUT) 114.

In operation, the DLL 106 is locked to the reference clock input "$Sref_0(t)$" such that "N" identical, but time shifted, versions of the reference clock are produced on the plurality of outputs of delay line 106. Each output or tap on the delay line is shifted by Tref/N, where Tref is the period of the reference clock. The "ith" tap on the delay line 106 can be described as:

$$Sref_i(t) = Sref_0(t - \frac{iTref}{N}).$$

The multiplexor 108 contains N inputs, one corresponding to each tap on the delay line. The synchronization circuit 110 gates the output 116 of the multiplexor 108 such that a pulse appears at the synchronization circuit's output port OUT 114 only when it is gated by a signal at input TRIG 112. The synchronization circuit 110 in accordance with the invention operates by creating a time aperture at the multiplexor output.

The timing diagram of FIG. 2 illustrates a time aperture in a first embodiment and also demonstrates two difficulties encountered with the DPC 100 in this first embodiment. The first problem with the time aperture is that, of necessity, the aperture has minimum time width Wref + Tref, where Wref is the width of the reference pulse. Note that Wref can be less than ½ of Tref in the embodiments of the present invention described herein. Because this time is longer than the period of the reference signal Tref, the pulse rate of the TRIG signal 112 is limited to less than the reference frequency of REF signal 102.

The second problem is that the time aperture is sufficiently wide that it can pass more than one pulse on a given signal, leading to an incorrect number of pulses in the converter output. A solution to this problem is used in a preferred embodiment to divide the time aperture into regions based on the value of the input signal. An example of this embodiment is shown in FIG. 3. In FIG. 3, two aperture regions are defined. For small IN 104 (IN <=N/2) the aperture begins on the first rising edge of the REF signal 102 after the first rising edge of the TRIG signal 112 and remains active for 3/2 Tref. For large IN (IN> N/2) the aperture begins on the first falling edge after the first rising edge of the REF signal 102 after a trigger signal and remains active for 3/2 cycle. For a mid-range signal (N = approximately N/2), only one pulse occurs during an aperture opening.

The present invention shown in FIG. 1 can be realized using existing circuit techniques. The tuned delay line 106 can preferably be designed using a DLL although other tuning approaches known in the art can be used. The multiplexor 108 is of a conventional design as is known in the art. The aperture can be realized with the sequential circuit 400 shown in FIG. 4 in accordance with the preferred embodiment of the present invention, which is shown as trigger (or synchronization) circuit 110 in FIG. 1. The INDEX (msb) signal 402 is the most significant bit of the DPC input (IN) 104. Note that the INDEX input 402 to the

synchronization circuit 110 is not shown in FIG. 1 in order to simplify the presentation. By narrowing the aperture window and gating its start time with information from the IN port 104 the tendency of the trigger circuit to pass multiple pulses through a single aperture window is solved. The points "A", "B", "C" and "E" on the top circuit of the sequential circuit 400 are connected to the their corresponding points on the lower circuit.

Although the preferred embodiment of DPC 100 has been described above, different variations of the invention can be done. For example, the delay line 106 can be implemented with an inverter chain where each inverter output represents a delay-line tap. In this third embodiment, the circuit is driven by a 50% duty cycle waveform and the multiplexor to delay line interface is ordered such that inverted versions of the input clock represent the input clock shifted by 180 degrees plus the time delay of the chain. This doubles the resolution of the circuit compared to a circuit with only non-inverted outputs used as taps.

Another embodiment of the present invention takes advantage of the periodic nature of the REF signal 102 and forms a delay line with multiple cycles of time delay. These multiple cycles of time delay can be used to increase resolution of the system. The delay-line to multiplexor interface in this

embodiment is ordered to take advantage of full-cycle delays. The number of taps and the number of cycles cannot have common factors. Taps must be ordered so fractional portion of delay increases monotonically as the tap position number increases. As an example of this approach, tap ordering for the case of 17 delay gates, and 4 clock cycles of delay is demonstrated in Table 1 below.

TABLE 1

Gate	Delay (as fraction of Tref)	Fractional portion of Delay (as fraction of Tref)	Tap position
1	4/17	4/17	4
2	8/17	8/17	8
3	12/17	12/17	12
4	16/17	16/17	16
5	20/17	3/17	3
6	24/17	7/17	7
7	28/17	11/17	11
8	32/17	15/17	15
9	36/17	2/17	2
10	40/17	6/17	6
11	44/17	10/17	10
12	48/17	14/17	14
13	52/17	1/17	1
14	56/17	5/17	5
15	60/17	9/17	9
16	64/17	13/17	13
17	68/17	0/17	0

While several embodiments of the invention have been illustrated and described, it will be clear that the invention is not so limited. Numerous modifications, changes, variations, substitutions and equivalents will occur to those skilled in the art without departing from the spirit and scope of the present

invention as defined by the appended claims. The present invention can be used in for example; Voltage-controlled-oscillator-less (VCO-less) frequency synthesizers and modulators for use in communication devices, instrumentation, etc.

What is claimed is:

CLAIMS

1. A digital-to-phase converter, comprising:

a delay line having a plurality of delay taps;

a multiplexor coupled to the delay line, the multiplexor having a plurality (N) of input ports for receiving the plurality of delay taps and an output port for providing an output signal; and

a synchronization circuit having a first input port for receiving the output signal from the multiplexor and a second input port for receiving a trigger signal, the synchronization circuit further having an output port for providing an output signal only when the synchronization circuit is gated by the trigger signal (TRIG).

2. A digital-to-phase converter as defined in claim 1, further comprising a reference clock signal having a time period and coupled to the delay line and the synchronization circuit, and wherein the delay line is tuned to a delay equal to the time period of the reference clock signal.

3. A digital-to-phase converter as defined in claim 1, wherein the plurality of delay taps on the delay line are equally spaced.

4. A digital-to-phase converter as defined in claim 1, wherein the delay line comprises an inverter chain where each inverter output represents a delay-line tap.

5. A digital-to-phase converter as defined in claim 4, further comprising a reference clock signal and the inverted version of the input clock signal represents the input clock shifted by 180 degrees plus the time delay of the delay line.

6. A digital-to-phase converter as defined in claim 1 wherein the delay line is slaved to a delay-line-loop (DLL).

7. A digital-to-phase converter as defined in claim 1, further comprising:

a reference clock providing a reference signal (REF) to the delay line and the synchronization circuit, and

the multiplexor includes an input port for receiving an n-bit binary word (IN).

8. A digital-to-phase converter as defined in claim 7, wherein the reference signal (REF) is a pulse train having rising and falling edges and the synchronization circuit forms multiple apertures that depend on the value of (IN).

9. A digital-to-phase converter as defined in claim 7, wherein the reference signal (REF) is a pulse train having rising and falling edges and the synchronization circuit forms an aperture region when IN <=N/2 that begins on the first rising edge of the reference signal (REF) after the first rising edge of the trigger signal (TRIG) signal and remains active for a predetermined period thereafter.

10. A digital-to-phase converter as defined in claim 9, wherein the predetermined period that the aperture region formed by the synchronization circuit remains active is approximately 3/2 the period (Tref) of the reference signal (REF).

11. A digital-to-phase converter as defined in claim 9, wherein the synchronization circuit forms an aperture region when IN >N/2 that begins on the first falling edge after the first rising edge of the reference signal (REF) after a trigger signal (TRIG) has occurred and the aperture region remains active for a predetermined period of time.

12. A digital-to-phase converter as defined in claim 11, wherein the predetermined period of time that the aperture remains active is for approximately 3/2 the period (Tref) of the reference signal.

13. A digital-to-phase converter, comprising:

a tuned delay line having a plurality of delay taps;

a multiplexor coupled to the delay line, the multiplexor having a plurality (N) of input ports for interconnecting with the plurality of delay taps on the tuned delay line and an output port for providing an output signal;

a synchronization circuit;

a reference clock providing a reference signal (REF) to the tuned delay line and the synchronization circuit; and

the delay line is tuned to a delay equal to the time period of the reference signal.

14. A digital-to-phase converter as defined in claim 13, wherein the delay line is adjusted using a delay-locked-loop (DLL).

15. A digital-to-phase converter as defined in claim 13, further comprising an output port coupled to the synchronization circuit and wherein the synchronization circuit provides a time aperture that allows the multiplexor's output signal to be presented at the output port of the synchronization circuit.

16. A digital-to-phase converter as defined in claim 13, wherein the delay taps are ordered so the fractional portion of the delay increases monotonically as the tap position number increases.

DIGITAL-TO-PHASE-CONVERTER

ABSTRACT OF THE DISCLOSURE

A digital-to-phase or digital-to-time-shift converter (100) includes a delay line (106), a multiplexor (108) and synchronization circuit (110). In the converter (100) the clock edges of a reference signal are shifted in response to the value of a multi-bit digital word, IN (104). The synchronization circuit (110) gates the output of the multiplexor (108) such that a pulse appears at the synchronization circuit's (110) output port (114) only when the circuit is gated by a signal at input TRIG (112). The synchronization circuit (110) creates a time aperture for the multiplexor output.

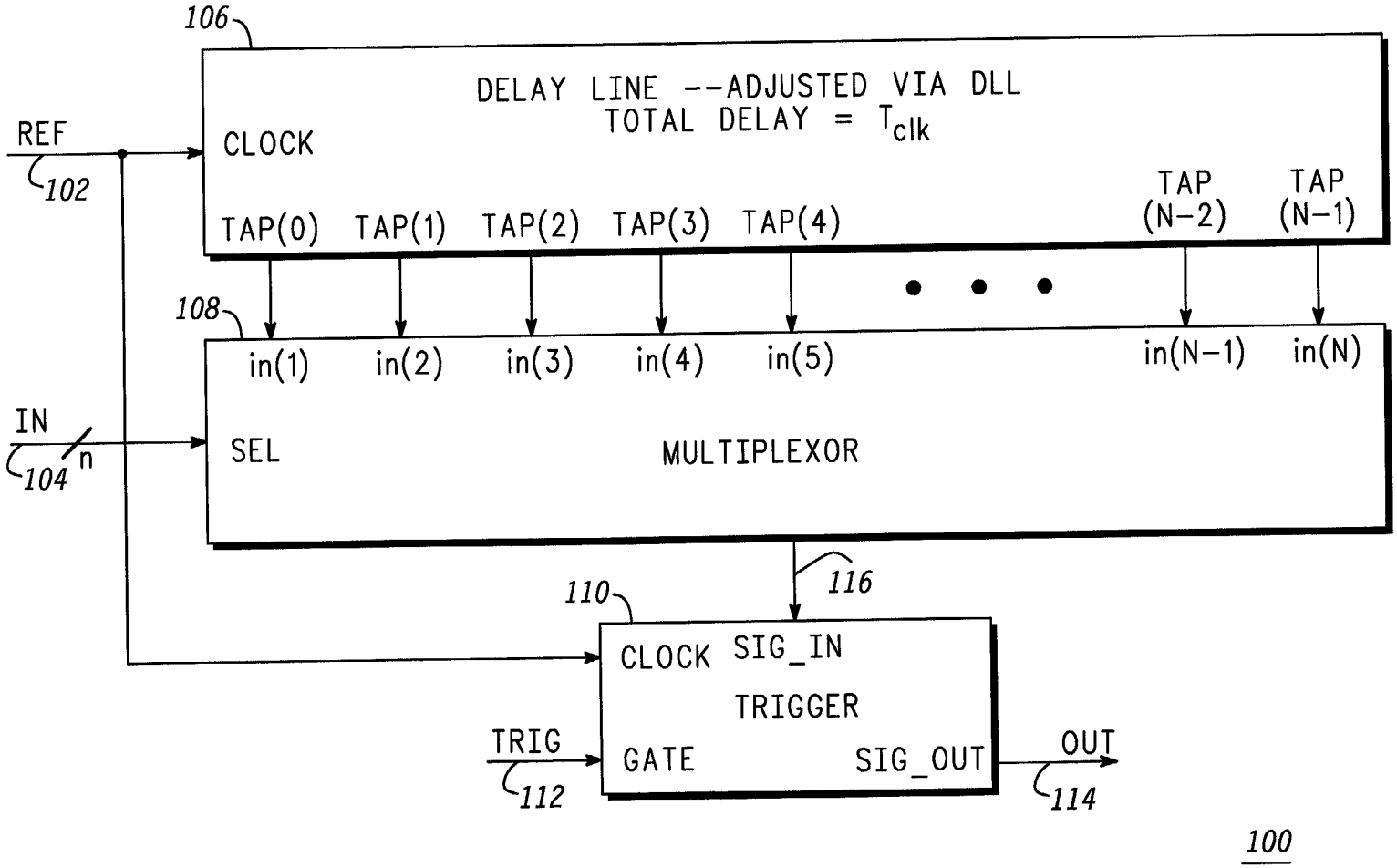

106
DELAY LINE --ADJUSTED VIA DLL
TOTAL DELAY = T_{clk}
REF
102
CLOCK
TAP(0) TAP(1) TAP(2) TAP(3) TAP(4)
TAP (N-2)
TAP (N-1)
108
in(1) in(2) in(3) in(4) in(5)
in(N-1) in(N)
IN
104
n
SEL
MULTIPLEXOR
116
110
CLOCK SIG_IN
TRIGGER
TRIG
112
GATE
SIG_OUT
OUT
114
100

FIG. 1

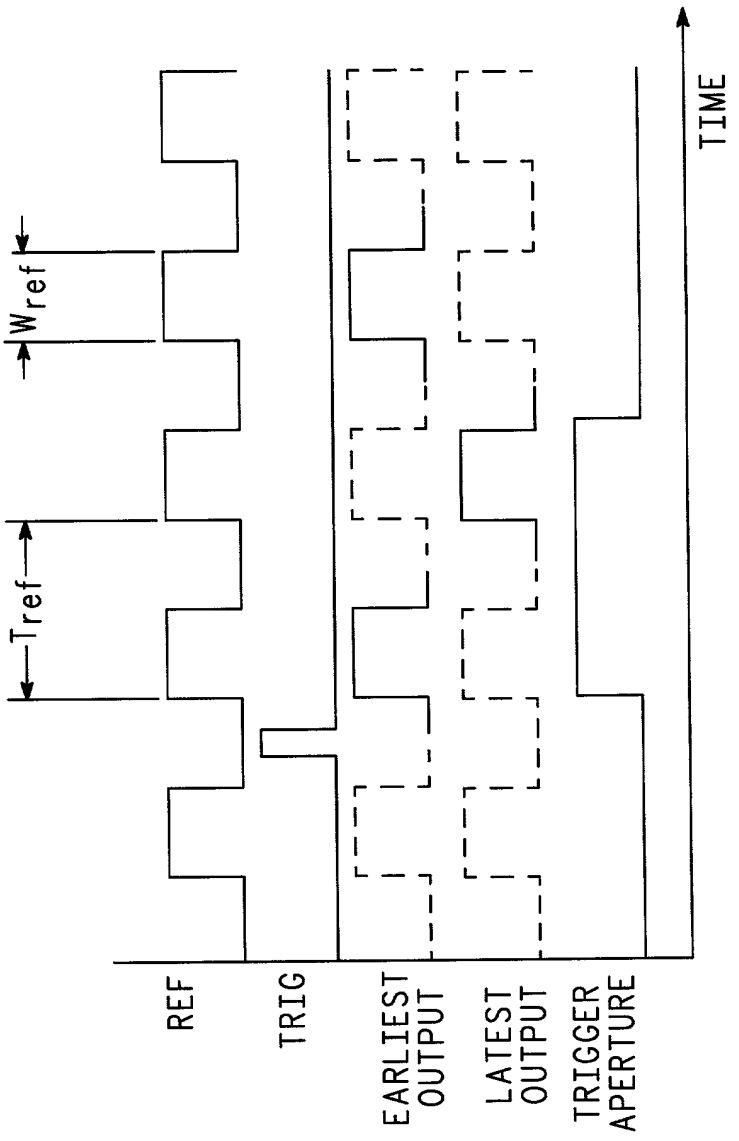

Tref
Wref
REF
TRIG
EARLIEST OUTPUT
LATEST OUTPUT
TRIGGER APERTURE
TIME

FIG. 2

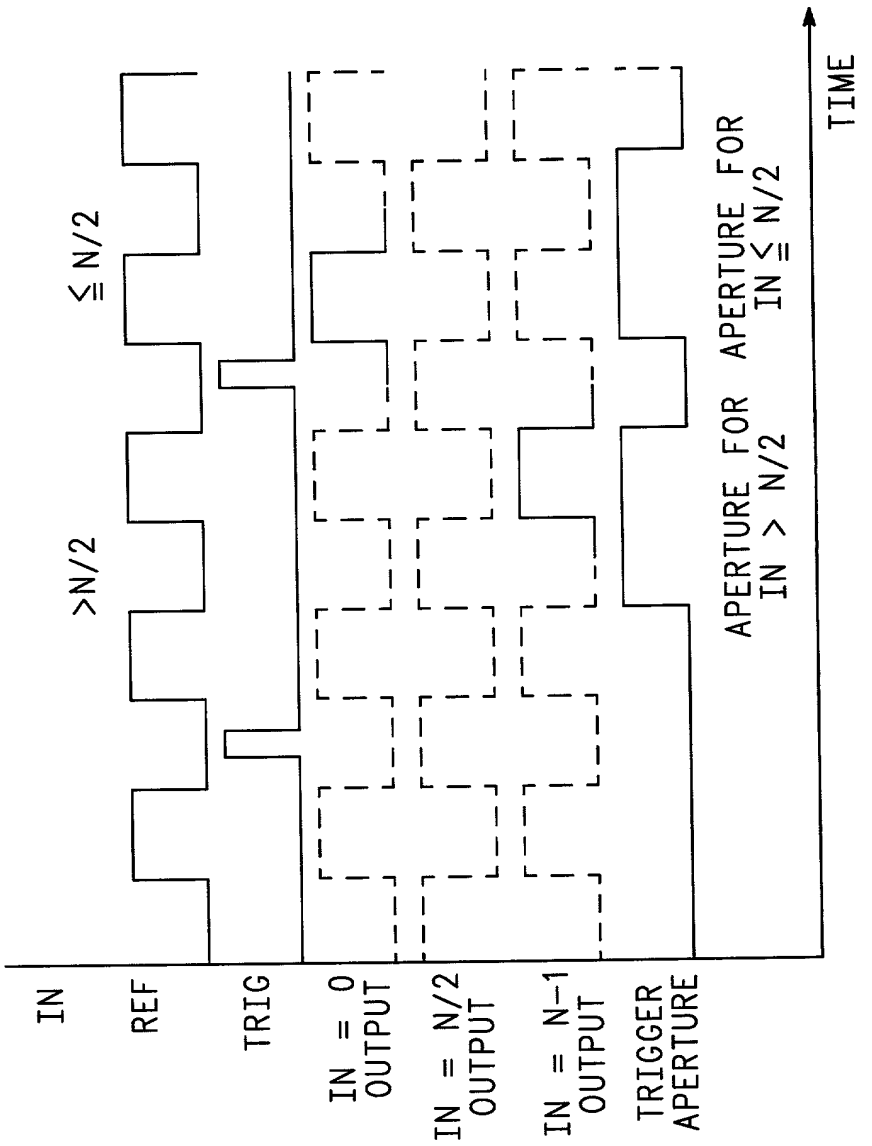

IN
REF
TRIG
IN = 0 OUTPUT
IN = N/2 OUTPUT
IN = N-1 OUTPUT
TRIGGER APERTURE
>N/2
≦N/2
APERTURE FOR IN > N/2
APERTURE FOR IN ≦ N/2
TIME

FIG. 3

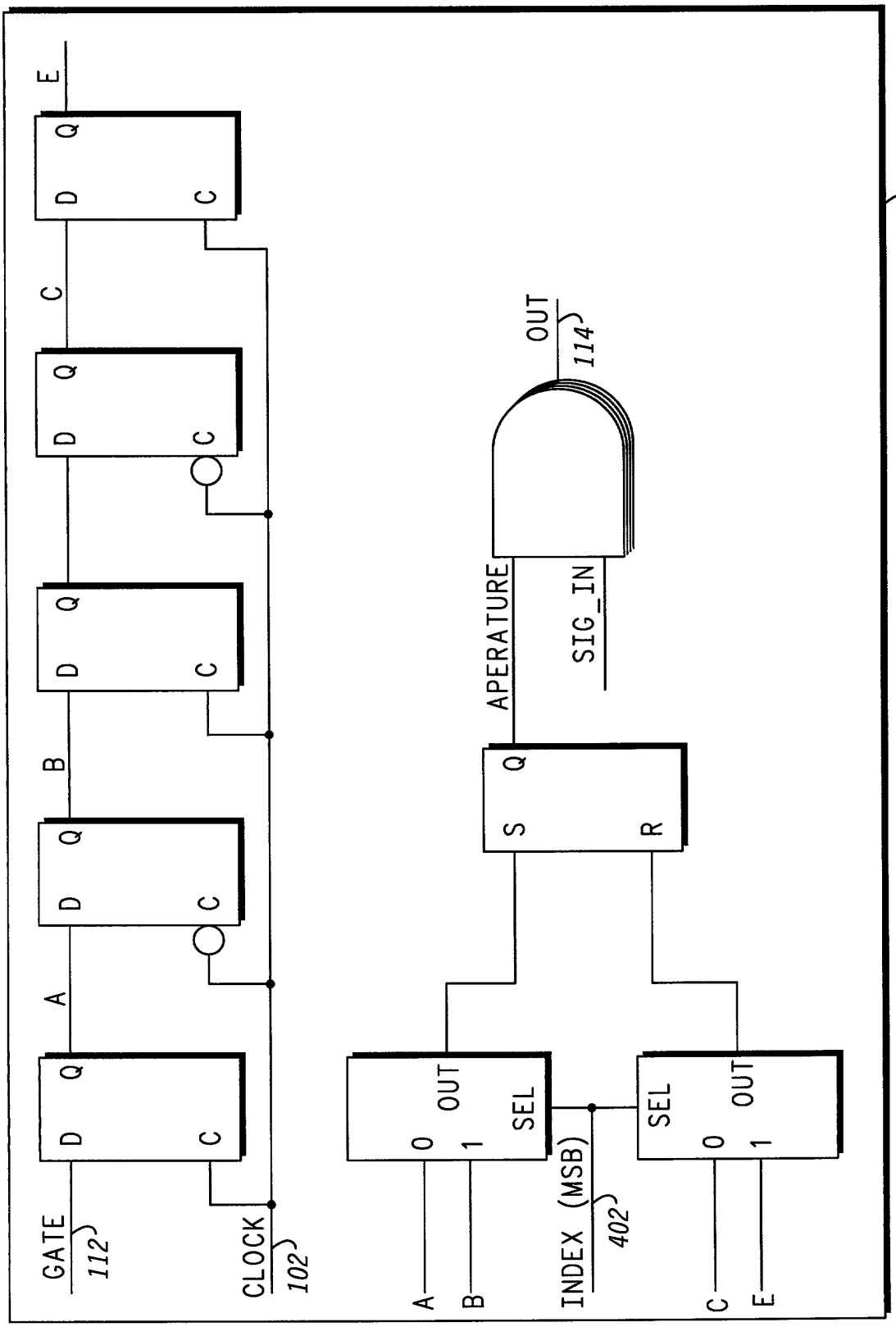

400
GATE
112
CLOCK
102
A
B
C
E
D
Q
C
OUT
114
APERATURE
SIG_IN
S
R
SEL
OUT
0
1
INDEX (MSB)
402

FIG. 4

PATENT APPLICATION DECLARATION
COMBINED WITH POWER OF ATTORNEY

Attorney's Docket No.: CM03054J

☒ Regular (Utility) ☐ Design Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DIGITAL-TO-PHASE-CONVERTER

the specification of which:

☒ is attached hereto ☐ was filed on: _____

as U.S. Serial No.: _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign/PCT Application(s):

☒ no such application(s) filed ☐ such application(s) identified as follows:

Application Number	Country	Date of Filing *(day, month, year)*	Priority Claimed Under 37 U.S.C. 119
			☐ Yes ☐ No
			☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Provisional Application Serial No.: _____

Provisional Application Filing Date: _____

I hereby claim the priority benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which is material to the patentability of this application and which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s):

☒ no such application(s) filed

☐ such application(s) identified as follows:

Application No.	Filing Date *(day, month, year)*	Status *(Patented, Pending, Abandoned)*

I hereby declare that: as to any claimed subject matter of this application which is common to my earlier United States or foreign application(s), if any, which I have identified above and claimed the benefit of priority thereof, I do not believe that the same was ever known or used in the United States before my invention thereof or patented or described in any printed publication in any country before my invention thereof or more than one year prior to the first of said earlier application(s), or in public use or on sale in the United States more than one year prior to the first of said earlier application(s), and that the said common subject matter has not been patented or made the subject of an inventor's certificate before the date of the first of said earlier U.S. application(s) in any country foreign to the United States on an application, filed by me or my legal representatives or assigns more than twelve months (six months if the present application is a Design patent application) prior to the first of said earlier U.S. application(s), if any; and that, as to any claimed subject matter of this application which is not common to said earlier application(s), if any, I do not know and do not believe that the same was ever known or used in the United States before my invention thereof or patented or described in any printed publication in any country before my invention thereof or more than one year prior to the date of this application, or in public use or on sale in the United States more than one year prior to the date of this application, and that said subject matter has not been patented or made the subject of an inventor's certificate in any country foreign to the United States on an application filed by me or my legal representatives or assigns more than twelve months (six months if the present application is a Design patent application) prior to the date of this application.

I HEREBY APPOINT THE ATTORNEY(S) OR AGENT(S) ASSOCIATED WITH:

CUSTOMER NUMBER 24273

TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH.

Address all telephone calls to:

James A. Lamb
Telephone: (954) 723-6449
Facsimile: (954) 723-3871

Address all correspondence to: Customer Number 24273

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first-named or sole inventor FREDERICK L. MARTIN

Inventor's signature Frederick L Martin Date 8/1/00

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Citizenship United States of America (Country)

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